Silicon On Insulator

Introduction

In an integrated circuit, the individual transistors must be isolated from each other for correct circuit operation. In most IC processes, this is done by using reverse biased PN junctions and the technology is referred to as Junction Isolation (JI). The degree of isolation is limited by collector-substrate leakage currents and voltage modulated collector-substrate capacitance. An ideal isolation technology would not have leakage and capacitive coupling between devices.

Intersil uses a Silicon On Insulator (SOI) bipolar process, which differs radically from conventional bipolar JI processes in that the individual transistors are electrically isolated from their neighbors by a layer of glass. With the Intersil SOI process, a layer of glass (SiO_2) surrounds the transistors on all four sides and the bottom. This totally isolates the individual transistors and provides essentially ideal isolation.

Silicon On Insulator (SOI) is a way of building monolithic integrated circuits, which have performance that rivals a multi-chip hybrid.

Intersil SOI Process

Intersil uses SOI to make both NPN transistors and PNP transistors in a high frequency vertical structure as shown in Figure 1. There are two collector, two base and two emitter diffusions. Therefore, each transistor type can be optimized without compromising its complement. In analog circuit design, both NPN and PNP transistors are in the signal path. Thus the slower of the two transistors determines the overall circuit speed limitations. Most JI processes use lateral structure PNP transistors, which have speed characteristics (f_t) that are 50 to 100 times slower than the NPNs. Thus most JI processes are 50 to 100 times slower than Intersil's SOI process.

SOI also has the capability of operating at a given high frequency with lower power consumption than conventional bipolar processes of similar geometry due to the reduced collector-substrate capacitance. These stray capacitances require extra supply current to charge them, supply current that is otherwise unnecessary in the circuit. Collector to substrate capacitances in SOI are about one-tenth of those in JI.

SOI is an isolation technique and as such is a process technology platform, which may be used as a starting point in more esoteric process development. Intersil's advanced SOI process today uses implanted resistors, MOS capacitors and Schottky diodes in addition to high performance, totally implanted complementary transistors. Other elements may be added such as BiFETS and thin film resistors. CMOS or even combined CMOS and bipolar (BiCMOS) can be implemented on SOI In all cases, the SOI lend its superb isolation, low leakage and high-speed characteristics to the process.

Intersil's patented SOI technology has been improved substantially from the original process. Performance and device density have been increased resulting in costs equaling that of standard JI Intersil's latest process has NPN and PNP Ft's of 4GHz at 40V, 2 micron CMOS and very low defect density.

SOI Benefits

Speed

Speed is improved in SOI integrated circuits for two reasons. First, since the collector substrate capacitance is smaller than JI by a factor of 10, the slew rate of an internal node can be 10 times as fast as the same node in JI, using the same amount of current. Second, it is very difficult to build fast vertical PNP transistors with JI, so most JI circuits settle for using a lateral PNP transistor somewhere in the signal path. With SOI, fully isolated fast vertical PNP and NPN transistors can be made on the same chip and therefore performance need not be compromised by a slow transistor.

Temperature Performance

All junctions have leakage currents directly impacted by temperature. Higher temperatures create higher leakages. Many integrated circuits stop working if stray leakages between adjacent transistors are too high. Thus at high temperatures, these ICs cease working. With SOI, the high temperature leakages between adjacent transistors do not exist and the circuit can continue to work at high temperatures. Applications such as oil wells, where the temperatures may reach +200°C, are prime examples where SOI is necessary for its temperature characteristics.

Radiation Hardness

The same leakages affected by temperature are also affected by radiation. The radiation may be from either a nuclear event or from deep space radiation. Because the SOI glass layer is unaffected by radiation, the performance of SOI circuits in the presence of radiation makes SOI the mandatory technology for many military applications.

Freedom From Latch-up

Many JI devices are prone to latch-up. That is, under some external conditions the circuit will become stuck in a particular internal condition and will not function properly until the power is removed. Sometimes the circuit will self destruct due to latch-up. A key factor in this latch-up is the participation of the isolation junction in the circuitry that creates a parasitic SCR (Silicon Controlled Rectifier). In SOI, since there is no isolation junction, there can be no latch-up.

Intersil SOI Advantages Over JI

- Speed
  - Fast (vertical) PNPs and NPNs
  - Lower Collector to substrate capacitance
  - Collector to substrate capacitance not modulated by collector voltage
- No Possibility of Circuit Latch-up via Parasitic SCRs
  - No parasitic devices with SOI
- Operates in High Temperature and Radiation Environments
  - Leakage currents are blocked by SOI walls
- High Voltage Operation
  - Device to device breakdown >2000V
- Mixed Technologies on Same Chip
  - Bipolar transistors, diffused resistors and MOS can be done on the same monolithic chip

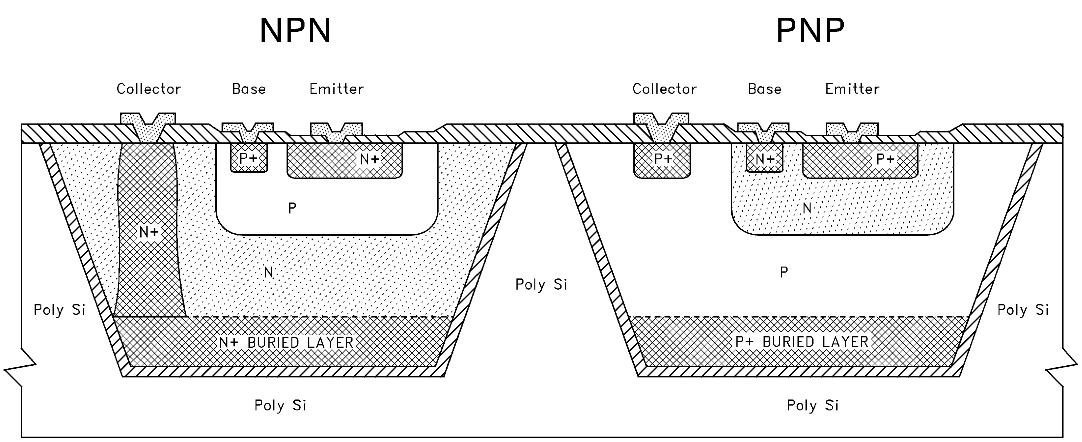

FIGURE 1. COMPLIMENTARY SOI PROCESS